



- L1: (76449) sdram or (synchronous adj2 (DRAM) or (dynamic adj3 memory))
- L2: (262) write adj recovery adj time
- L3: (336) precharge adj3 ((row adj3 strobe) or RAS)
- L4: (62850) clock adj2 frequency
- L6: (1) 2 same 3
- L6: (13) 2 same 4
- L7: (1806) precharge adj2 time
- L12: (10) 2 same 7
- L14: (2198) delay\$4 with precharg\$4
- L15: (34) 2 and 14
- L18: (6) (first or second) adj2 2
- L19: (2762) (precharg\$4 or pre-charg\$4) adj2 time
- L20: (21) 2 same 19
- L24: (16348) ddr or (double adj data adj rate)
- L25: (2701) (first or second) adj2 4
- L26: (8) 24 same 26
- L27: (64) 24 and 26
- L29: (66) (precharg\$4 or pre-charge\$4) with 2
- L30: (1) 25 and 29
- L31: (8) 24 and 29
- L32: (32) 29 not (31 or 26 or 27 or 20 or 16)
- L33: (2649) 366/194
- L34: (6542) 366/233
- L35: (6037) 366/203
- L36: (84370) "366"/\$6
- L37: (29) 2 and 33
- L38: (60) 2 and 34
- L39: (63) 2 and 36
- L40: (92) 37 or 38 or 39
- L42: (31) 19 and 40
- L43: (162) 2 and 36
- L45: (12) (JACUNSKI near2 MARK).in.
- L46: (62) (NORRIS near2 ALAN).in.
- L47: (6) (WEINSTEIN near2 SAMUEL).in.

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 Default operator: OR Highlight hit terms initially

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	?	3
1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20030186076 A1	20031002	23	Auto-precharge control circuit	366/203			Park, Sang-Kyun et al.	<input type="checkbox"/>				
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6353573 B1	20020306	26	Clock synchronization semicon	366/233	366/194		Koshikawa; Yasuji	<input type="checkbox"/>				
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6434082 B1	20020813	21	Clocked memory device that in	366/233	366/203		Hovis; William Paul et al.	<input type="checkbox"/>				
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6507526 B2	20030114	10	Semiconductor memory with im	366/203	366/194		Otake; Hiroyuki	<input type="checkbox"/>				

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